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PATENT

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| Applicant: | KUO et al. | Examiner: | BORKOWSKI, R. |
| Serial No.: | 10/760,019 | Group Art Unit: | 2181 |
| Filed: | January 16, 2004 | Docket No.: | **SJO920030027US1** (IBMS.070-0511) |
| Title: | METHOD, APPARATUS AND PROGRAM STORAGE DEVICE FOR MANAGING DATAFLOW THROUGH A PROCESSING SYSTEM | | |

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Mail Stop Appeal, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 24, 2006.

By: David W. Lynch

## APPEAL BRIEF

Mail Stop Appeal
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Appeal Brief submitted pursuant to 37 C.F.R. § 41.37 for the above-referenced patent application. Please charge Deposit Account No. 09-0466 (**SJO920030027US1**) in the amount of $500.00 for this brief in support of appeal as indicated in 37 C.F.R. § 41.20(b)(2).

10/31/2006 HDEMESS1 00000002 090466 10760019
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11/01/2006 HDEMESS1 00000004 090466 10760019
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### C. Conclusion

In view of the above, Appellant submits that the rejections are improper, the claimed invention is patentable, and that the rejections of claims 1-29 should be reversed. Appellant respectfully requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Respectfully submitted,

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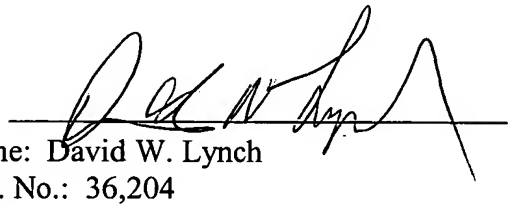
By: 
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## I. Real Party In Interest

The real party in interest is International Business Machines Corporation, having a place of business at New Orchard Road, Armonk, New York 10504. This application is assigned to International Business Machines Corporation.

## II. Related Appeals And Interferences

Appellant is unaware of any related appeals, interferences or judicial proceedings.

## III. Status Of Claims

Claims 1-29 are rejected. Claims 1-29 are presented for appeal and may be found in the attached Appendix of Appealed Claims in their present form.

## IV. Status Of Amendments

No amendments to the claims were made subsequent to the final rejection of Appellants' application.

## V. Summary Of Claimed Subject Matter

Appellant's invention is a method, apparatus and program storage device for managing dataflow through a processing system.

Claim 1 is directed to a method for managing dataflow through a processing system. The method includes gathering writes in a buffer before transmitting a burst of writes over an external bus (Fig. 3, 330; page 13, lines 10-11), monitoring the buffer to determine a number of writes in the buffer (Fig. 3, 340; page 13, lines 12-13) and whether the number of writes in the buffer exceed a predetermined threshold (Fig. 3, 346; page 13, lines 15-16), identifying an error condition (Fig. 3, 350; page 13, lines 17-18) when the number of writes in the buffer exceed the predetermined threshold and providing control over a rate of a number of writes (Fig. 3, 324; page 13, lines 18-19) provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold.

Claim 11 is directed to a processing system. The processing system includes a processor (Fig. 3, 324; page 13, lines 18-19) for generating writes over a processor bus, a buffer (Fig. 3, 330; page 13, lines 10-11), coupled to the processor bus, for gathering the writes before transmitting a burst of writes over an external bus (Fig. 3, 330; page 13, lines 10-11) and a bus monitor (Fig. 3, 340; page 13, lines 12-13), coupled to the write buffer, for determining a number of writes in the buffer, identifying an error condition when the number of writes in the buffer exceed the predetermined threshold (Fig. 3, 346; page 13, lines 15-16), and providing control over a rate of a number of writes provided to the buffer (Fig. 3, 324; page 13, lines 18-19) in response to the monitored number of writes in the buffer and the predetermined threshold.

Claim 27 is directed to another embodiment of a processing system. The processing system includes a memory (Fig. 3, 330; page 13, lines 10-11) for gathering writes for burst transmission over an external bus and a processor (Fig. 3, 324; page 13, lines 18-19), coupled to the memory, the processor being configured for monitoring the memory to determine a number of writes in the buffer (Fig. 3, 340; page 13, lines 12-13) and whether the number of writes in the memory exceed a predetermined threshold (Fig. 3, 346; page 13, lines 15-16), identifying an error condition when the number of writes in the buffer exceed the predetermined threshold (Fig. 3, 346; page 13, lines 15-16), and providing control over a rate of a number of writes provided to the memory (Fig. 3, 324; page 13, lines 18-19) in response to the monitored number of writes in the memory and the predetermined threshold.

Claim 28 is directed to a program storage device (Fig. 5, 568; page 15, lines 9-12) readable by a computer, the program storage device tangibly embodying one or more programs of instructions (Fig. 5, 590; page 15, lines 16-19) executable by the computer to perform a method for managing dataflow through a processing system. The method includes gathering writes in a buffer before transmitting a burst of writes over an external bus (Fig. 3, 330; page 13, lines 10-11), monitoring the buffer to determine a number of writes in the buffer (Fig. 3, 340; page 13, lines 12-13) and whether the number of writes in the buffer exceed a predetermined threshold (Fig. 3, 346; page 13, lines 15-16), identifying an error condition (Fig. 3, 350; page 13, lines 17-18) when the number of writes in the buffer exceed the predetermined threshold and providing control over a rate of a number of writes (Fig. 3, 324; page 13, lines 18-19) provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold.

Claim 29 is directed to another embodiment of a processing system. The processing system includes means (Fig. 3, 330; page 13, lines 10-11) for gathering writes for burst transmission over an external bus and means (Fig. 3, 340; page 13, lines 12-13), coupled to the means for gathering, for monitoring the means for gather to determine a number of writes in the buffer (Fig. 3, 340; page 13, lines 12-13) and whether the number of writes in the means for gathering exceed a predetermined threshold (Fig. 3, 346; page 13, lines 15-16), for identifying an error condition (Fig. 3, 350; page 13, lines 17-18) when the number of writes in the buffer exceed the predetermined threshold, and for providing control over a rate of a number of writes (Fig. 3, 324; page 13, lines 18-19) provided to the means for gathering in response to the monitored number of writes in the buffer and the predetermined threshold.

## VI. Grounds Of Rejections To Be Reviewed On Appeal

Appellant has attempted to comply with new rule 37 C.F.R. § 41.37(c) by providing the Office Action's grounds of rejection verbatim, followed by an argument section corresponding thereto.

**A. Claims 1-9, 11-25 and 27-29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Richardson in view of Collier.**

**B. Claims 10 and 26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Richardson and Collier in view of Azevedo et al.**

## VII. Argument

### A. REJECTION OF CLAIMS 1-9, 11-25 AND 27-29 UNDER 35 U.S.C. § 103(A) AS BEING UNPATENTABLE OVER RICHARDSON IN VIEW OF COLLIER

#### 1. INDEPENDENT CLAIMS 1, 11, 27, 28 AND 29 ARE PATENTABLE OVER RICHARDSON AND COLLIER

##### i. RICHARDSON FAILS TO TEACH, DISCLOSE OR SUGGEST MONITORING THE BUFFER TO DETERMINE A NUMBER OF WRITES IN THE BUFFER AND WHETHER THE NUMBER OF WRITES IN THE BUFFER EXCEED A PREDETERMINED THRESHOLD

The Final Office Action stated that Richardson disclosed gathering writes in a buffer, monitoring the buffer to determine the number of writes in the buffer and whether the number of writes in the buffer exceeds a predetermined threshold.

However, Richardson does not teach, disclose or suggest determining the number of writes in the buffer and whether the number of writes in the buffer exceeds a predetermined threshold. Rather, Richardson discloses a bus request queue (BRQ) for storing speculative write-combine (SWC) requests. Richardson uses a counter to maintain a count of the number

of SWC requests that are maintained in the BRQ. When an address of a new SWC request falls within the address range of a previously stored SWC request, the new SWC request is merged into the existing one (so the data can be combined in a single write). If a new BRQ entry is not allocated, the counter is not incremented.

If, on the other hand, the address of the new SWC request does not fall within the address range of stored SWC requests, the SWC request is stored in a new BRQ entry.

Richardson then discloses that the BIU holds each entry of SWC requests in the BRQ until its release is triggered by the occurrence of a special event. For example, release of a SWC request may be triggered when the counter value indicates that the number of independently maintained SWC requests having an address that does not fall within the address range of other stored SWC exceeds a threshold.

Nevertheless, Richardson does not monitor the buffer to determine the number of writes in the buffer. Further, Richardson does not disclose determining whether the number of writes in the buffer exceeds a predetermined threshold. Richardson is only concerned with the number of independently maintained BRQ entries of SWC requests as reflected by the counter in Richardson.

Accordingly, independent claims 1, 11 and 27-29 are patentable over Richardson.

### ii. RICHARDSON FAILS TO TEACH, DISCLOSE OR SUGGEST IDENTIFYING AN ERROR CONDITION WHEN THE NUMBER OF WRITES IN THE BUFFER EXCEED THE PREDETERMINED THRESHOLD

Richardson fails to even mention an error condition. In fact, the Final Office Action inherently admits that Richardson fails to mention identifying an error condition because the Final Office Action does not even address this limitation.

Still further, Richardson fails to disclose, teach or suggest identifying an error condition when the number of writes in the buffer exceeds the predetermined threshold. As described above, Richardson does not does not monitor the buffer to determine the number of writes in the buffer. Further, Richardson does not disclose determining whether the number of writes in the buffer exceeds a predetermined threshold. Richardson is only concerned with the number of independently maintained BRQ entries of SWC requests as reflected by the counter in Richardson.

Accordingly, independent claims 1, 11 and 27-29 are patentable over Richardson.

### iii. RICHARDSON AND COLLIER, ALONE OR IN COMBINATION, FAIL TO TEACH, DISCLOSE OR SUGGEST PROVIDING CONTROL OVER A RATE OF A NUMBER OF WRITES PROVIDED TO THE BUFFER IN RESPONSE TO THE MONITORED NUMBER OF WRITES IN THE BUFFER AND THE PREDETERMINED THRESHOLD

The Final Office Action admits that Richardson fails to disclose providing control over a rate of a number of writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold. However, the Final Office Action maintains that Collier discloses providing control over a rate of a number of writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold.

Appellant respectfully disagrees. Collier discloses a sending device that initially sends an amount of data to a receiving device, wherein the amount of data is chosen to fill the buffer at the receiving device. Then, the sending device halts further transmission until the receiving device sends a flow control packet to the sending device, wherein the flow

control packet indicates an available amount of free space in the buffer at the receiving device.

The receiving device monitors the buffer. When the amount of "free space" in the buffer exceeds a threshold, the receiving device transmits the flow control packet to the sending device.

Accordingly, Collier does not suggest controlling a rate of the number of writes provided to the buffer in response to the number of writes in the buffer

## 2. DEPENDENT CLAIM 2 IS PATENTABLE OVER RICHARDSON AND COLLIER

Claim 2 recites that control is further provided by slowing writes to the buffer when the writes in the buffer exceed the predetermined threshold. However, Richardson and Collier, alone or in combination, fail to disclose, teach or suggest slowing writes to the buffer when the writes in the buffer exceed the predetermined threshold.

As described above, both Richardson and Collier fail to suggest monitoring the buffer to determine the number of writes in the buffer. Accordingly, Richardson and Collier fail to suggest slowing writes to the buffer when the writes in the buffer exceed the predetermined threshold.

Therefore, Appellant respectfully submits that claim 2 is patentable over Richardson and Collier.

### 3. DEPENDENT CLAIM 4 IS PATENTABLE OVER RICHARDSON AND COLLIER

Claim 2 recites that error recovery is initiated in response to the writes in the buffer exceeding the predetermined threshold. However, Richardson and Collier, alone or in combination, fail to disclose, teach or suggest initiating error recovery in response to the writes in the buffer exceeding the predetermined threshold.

As described above, both Richardson and Collier fail to suggest monitoring the buffer to determine the number of writes in the buffer. Accordingly, Richardson and Collier fail to suggest initiating error recovery in response to the writes in the buffer exceeding the predetermined threshold.

Therefore, Appellant respectfully submits that claim 4 is patentable over Richardson and Collier.

### 4. DEPENDENT CLAIMS 6 AND 19 ARE PATENTABLE OVER RICHARDSON AND COLLIER

Claims 6 and 19 recite that control is provided over a rate of a number of writes provided to the buffer by providing a vector to a register and scanning the register for the vector to determine when a number of writes in the buffer is static and to slow writes to the buffer in response thereto. However, Richardson and Collier, alone or in combination, fail to disclose, teach or suggest control is provided over a rate of a number of writes provided to the buffer by providing a vector to a register and scanning the register for the vector to determine when a number of writes in the buffer is static and to slow writes to the buffer in response thereto.

Rather, Collier discloses using a bit in a register to indicate that a flow control packet should be sent. Collier also discloses that a device that sends enough data to fill the buffer at the

receiving device will stop sending data unless it learns of free space in the buffer. However, Collier fails to suggest determining when a number of writes in the buffer is static and slowing writes in response thereto. Collier simple stops sending data until a flow control packet is received indicating free space in the buffer at the receiving device.

Accordingly, Richardson and Collier, alone or in combination, fail to suggest providing a vector to a register and scanning the register for the vector to determine when a number of writes in the buffer is static and to slow writes to the buffer in response thereto.

Therefore, Appellant respectfully submits that claims 6 and 19 are patentable over Richardson and Collier.

## 5. DEPENDENT CLAIMS 7 AND 20 ARE PATENTABLE OVER RICHARDSON AND COLLIER

Claims 7 and 20 recite that a vector is provided to a register by asserting an interrupt line to the register to provide an indication of an almost full state for the buffer in response to the vector. However, as described above, Richardson and Collier, alone or in combination fail to suggest providing a vector to a register and scanning the register for the vector to determine when a number of writes in the buffer is static and to slow writes to the buffer in response thereto. Accordingly, Richardson and Collier fail to suggest providing a vector to a register by asserting an interrupt line to the register to provide an indication of an almost full state for the buffer in response to the vector.

Therefore, Appellant respectfully submits that claims 7 and 20 are patentable over Richardson and Collier.

## 6. DEPENDENT CLAIMS 8 AND 25 ARE PATENTABLE OVER RICHARDSON AND COLLIER

Claims 7 and 20 recite that the buffer is cleared when the writes in the buffer exceed the predetermined threshold. However, as described above, Richardson does not teach, disclose or suggest determining the number of writes in the buffer and whether the number of writes in the buffer exceeds a predetermined threshold. Rather, Richardson is only concerned with the number of independently maintained BRQ entries of SWC requests as reflected by the counter in Richardson.

Accordingly, Richardson does not suggest clearing the buffer when the writes in the buffer exceed the predetermined threshold.

Collier fails to remedy the deficiencies of Richardson. Also as described above, Collier merely discloses a sending device that initially sends an amount of data to a receiving device, wherein the amount of data is chosen to fill the buffer at the receiving device. Then, the sending device halts further transmission until the receiving device sends a flow control packet to the sending device, wherein the flow control packet indicates an available amount of free space in the buffer at the receiving device.

The receiving device monitors the buffer. When the amount of "free space" in the buffer exceeds a threshold, the receiving device transmits the flow control packet to the sending device.

Accordingly, Richardson and Collier, alone or in combination, fail to suggest clearing the buffer when the writes in the buffer exceed the predetermined threshold.

### 7. DEPENDENT CLAIM 9 IS PATENTABLE OVER RICHARDSON AND COLLIER

Claim 9 recites that a timeout signal is provided for indicating when a transaction is not cleared from the buffer within a predetermined amount of time and clearing the buffer and external bus transactions in response thereto. Collier merely describes sending a flow control packet at predetermined time intervals. However, Collier does not mention providing a timeout signal when transactions are not cleared form the buffer within a predetermined period of time.

Accordingly, Richardson and Collier, alone or in combination, fail to suggest providing a timeout signal for indicating when a transaction is not cleared from the buffer within a predetermined amount of time and clearing the buffer and external bus transactions in response thereto.

## B. CLAIMS 10 AND 26 WERE REJECTED UNDER 35 U.S.C. § 103(A) AS BEING UNPATENTABLE OVER RICHARDSON AND COLLIER IN VIEW OF AZEVEDO ET AL.

### 1. DEPENDENT CLAIM 10 IS PATENTABLE OVER RICHARDSON AND COLLIER IN VIEW OF AZEVEDO ET AL.

Claim 10 recites that a determination is made whether an external interface is hung based upon detecting a static buffer pointer representing a lack of movement of writes in the buffer and clearing the buffer and external bus transactions when an external interface is hung. The Final Office Action admits that Richardson and Collier fail to disclose, teach or suggest determining whether an external interface is hung based upon detecting a static buffer pointer representing a lack of movement of writes in the buffer and clearing the buffer and external bus transactions when an external interface is hung.

Azevedo et al. fail to remedy the deficiencies of Richardson and Collier. Azevedo et al. merely discloses circuitry that times each pending request of a control master for the shared bus. Azevedo et al. initiates bus recovery when the control master exceeds a pre-determined time period allowed for waiting to acquire the shared bus control and complete the transfer on the shared bus.

Azevedo does not monitor the number of writes in a buffer. Rather, Azevedo merely monitors a time period allowed for acquiring a shared bus control and completing the transfer on the shared bus. Azevedo does not suggest detecting a static buffer pointer. Instead Azevedo et al. merely monitors a time period allowed for a control master to wait for the bus.

Accordingly, Richardson, Collier and Azevedo et al., alone or in combination, fail to disclose, teach or suggest determining whether an external interface is hung based upon detecting a static buffer pointer representing a lack of movement of writes in the buffer.

Therefore, Appellant respectfully submits that claim 10 is patentable over Richardson, Collier and Azevedo et al.

## VIII. Claims Appendix

1. (Previously Presented) A method for managing dataflow through a processing system, comprising:

gathering writes in a buffer before transmitting a burst of writes over an external bus;

monitoring the buffer to determine a number of writes in the buffer and whether the number of writes in the buffer exceed a predetermined threshold;

identifying an error condition when the number of writes in the buffer exceed the predetermined threshold; and

providing control over a rate of a number of writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold.

2. (Original) The method of claim 1, wherein the providing control further comprises slowing writes to the buffer when the writes in the buffer exceed the predetermined threshold.

3. (Original) The method of claim 1, wherein the gathering writes in a buffer before transmitting a burst of writes over an external bus further comprises transmitting a burst of writes over a bus.

4. (Original) The method of claim 1 further comprising initiating error recovery in response to the writes in the buffer exceeding the predetermined threshold.

5. (Original) The method of claim 1 further comprising providing an arbitration signal for controlling access to the external bus in response to the comparison of the writes in the buffer to the predetermined threshold.

6. (Previously Presented) The method of claim 1, wherein the providing control over a rate of a number of writes provided to the buffer further comprises providing a vector to a register and scanning the register for the vector to determine when a number of writes in the buffer is static and to slow writes to the buffer in response thereto.

7. (Original) The method of claim 6, wherein the providing a vector to a register further comprises asserting an interrupt line to the register to provide an indication of an almost full state for the buffer in response to the vector.

8. (Original) The method of claim 1 further comprising clearing the buffer when the writes in the buffer exceed the predetermined threshold.

9. (Original) The method of claim 1 further comprising providing a timeout signal for indicating when a transaction is not cleared from the buffer within a predetermined amount of time and clearing the buffer and external bus transactions in response thereto.

10. (Previously Presented) The method of claim 1 further comprising determining whether an external interface is hung based upon detecting a static buffer pointer representing a lack of movement of writes in the buffer and clearing the buffer and external bus transactions when an external interface is hung.

11. (Previously Presented) A processing system, comprising:

a processor for generating writes over a processor bus;

a buffer, coupled to the processor bus, for gathering the writes before transmitting a burst of writes over an external bus; and

a bus monitor, coupled to the write buffer, for determining a number of writes in the buffer, identifying an error condition when the number of writes in the buffer exceed the predetermined threshold, and providing control over a rate of a number of writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold.

12. (Original) The processing system of claim 11 further comprising an external interface coupled to the buffer, the external interface linking the buffer to the external bus.

13. (Original) The processing system of claim 11, wherein the external bus comprises a PCI-X bus.

14. (Original) The processing system of claim 11 further comprising a processor interface coupled to the buffer, the processor interface linking the buffer to a processor bus.

15. (Original) The processing system of claim 11, wherein the processor initiates error recovery in response to the writes in the buffer exceeding the predetermined threshold.

16. (Original) The processing system of claim 11, wherein the buffer monitor provides an arbitration signal for controlling access to an external bus in response to the comparison of the writes in the buffer to the predetermined threshold.

17. (Original) The processing system of claim 11, wherein the buffer monitor comprises bus arbitration and control logic for controlling the movement of data onto the external bus.

18. (Original) The processing system of claim 17, wherein the buffer bursts the writes onto the external bus.

19. (Previously Presented) The processing system of claim 11 further comprising a register, the buffer monitor providing a vector to the register, the processor scanning the register for the vector to determine when a number of writes in the buffer is static and to slow writes to the buffer in response thereto.

20. (Original) The processing system of claim 19, wherein the buffer monitor provides the vector by asserting an interrupt line to the register to provide an indication of an almost full state for the buffer.

21. (Original) The processing system of claim 19, wherein the vector represents an almost full state for the buffer.

22. (Original) The processing system of claim 11, wherein the buffer monitor monitors the buffer, the external bus, and the processor bus for error conditions.

23. (Previously Presented) The processing system of claim 22, wherein the error conditions comprise anticipated error conditions based upon detecting a static buffer pointer representing a lack of movement of writes in the buffer.

24. (Original) The processing system of claim 11, wherein the buffer monitor provides a buffer pointer to the processor to control the movement of writes from the processor to the buffer.

25. (Original) The processing system of claim 11, wherein the processor clears the buffer when the writes in the buffer exceed the predetermined threshold.

26. (Original) The processing system of claim 11, wherein the buffer monitor comprises a timer for providing a timeout signal to the processor when a transaction on the processor bus is not cleared within a predetermined amount of time.

27. (Previously Presented) A processing system, comprising:

a memory for gathering writes for burst transmission over an external bus; and

a processor, coupled to the memory, the processor being configured for monitoring the memory to determine a number of writes in the buffer and whether the number of writes in the memory exceed a predetermined threshold, identifying an error condition when the number of writes in the buffer exceed the predetermined threshold, and providing control over a rate of a number of writes provided to the memory in response to the monitored number of writes in the memory and the predetermined threshold.

28. (Previously Presented) A program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform a method for managing dataflow through a processing system, the method comprising:

gathering writes in a buffer before transmitting a burst of writes over an external bus;

monitoring the buffer to determine a number of writes in the buffer and whether the number of writes in the buffer exceed a predetermined threshold;

identifying an error condition when the number of writes in the buffer exceed the predetermined threshold; and

providing control over a rate of a number of writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold.

29. (Previously Presented) A processing system, comprising:

means for gathering writes for burst transmission over an external bus; and

means, coupled to the means for gathering, for monitoring the means for gather to determine a number of writes in the buffer and whether the number of writes in the means for gathering exceed a predetermined threshold, for identifying an error condition when the number of writes in the buffer exceed the predetermined threshold, and for providing control over a rate of a number of writes provided to the means for gathering in response to the monitored number of writes in the buffer and the predetermined threshold.

## IX. Evidence Appendix

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

## X. Related Proceedings Appendix

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.